

DATA SHEET

BSP130

N-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical
D-MOS transistor

BSP130

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

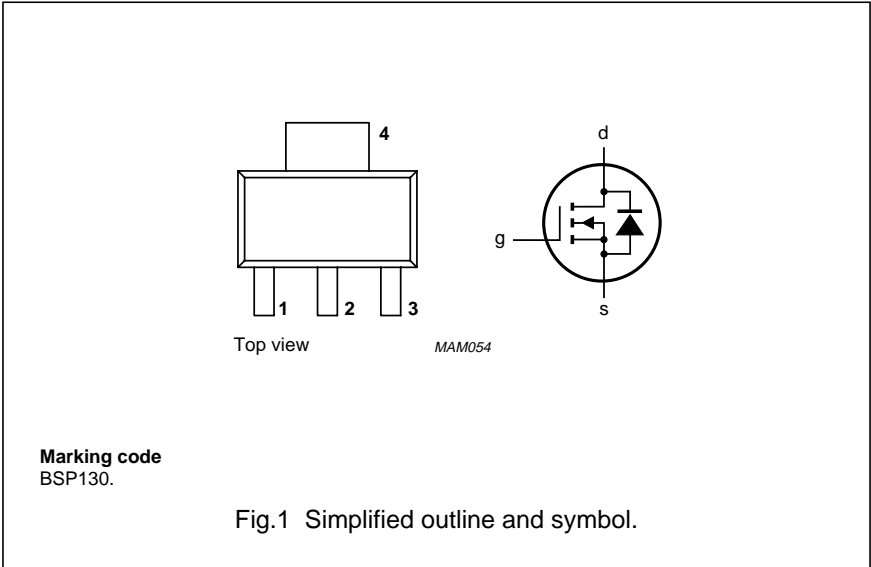
N-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a line current interruptor in telephone sets and for applications in relay, high-speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
I_D	DC drain current		–	300	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ }^{\circ}\text{C}$	–	1.5	W
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 250\text{ mA};$ $V_{GS} = 10\text{ V}$	–	8	Ω
$V_{GS(off)}$	gate-source cut-off voltage	$I_D = 1\text{ mA};$ $V_{DS} = V_{GS}$	0.8	2	V



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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	300	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
I_D	DC drain current		–	300	mA
I_{DM}	peak drain current		–	1.4	A
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ }^{\circ}\text{C}$; note 1	–	1.5	W
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	junction temperature		–	150	$^{\circ}\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient; note 1	83.3 K/W

Note

- Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\text{ }\mu\text{A}$; $V_{GS} = 0$	300	–	–	V
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}$; $V_{DS} = 0$	–	–	100	nA
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DS(on)}$	drain-source on-resistance	$I_D = 20\text{ mA}$; $V_{GS} = 2.4\text{ V}$	–	7.9	14	Ω
		$I_D = 250\text{ mA}$; $V_{GS} = 10\text{ V}$	–	6.7	8	Ω
I_{DSS}	drain-source leakage current	$V_{DS} = 240\text{ V}$; $V_{GS} = 0$	–	–	100	nA
$ Y_{fs} $	transfer admittance	$I_D = 250\text{ mA}$; $V_{DS} = 25\text{ V}$	200	380	–	mS
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	57	90	pF
C_{oss}	output capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	15	30	pF
C_{rss}	feedback capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0$; $f = 1\text{ MHz}$	–	2.6	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	$I_D = 250\text{ mA}$; $V_{DD} = 50\text{ V}$; $V_{GS} = 0\text{ to }10\text{ V}$	–	2.5	10	ns
t_{off}	turn-off time	$I_D = 250\text{ mA}$; $V_{DD} = 50\text{ V}$; $V_{GS} = 10\text{ to }0\text{ V}$	–	17	30	ns

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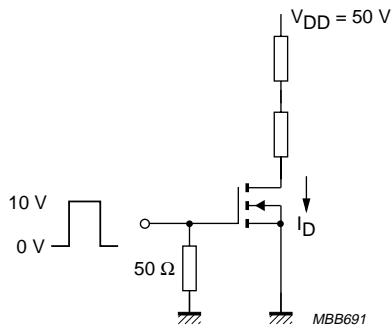


Fig.2 Switching times test circuit.

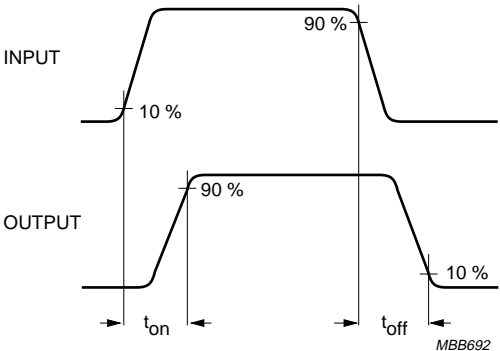


Fig.3 Input and output waveforms.

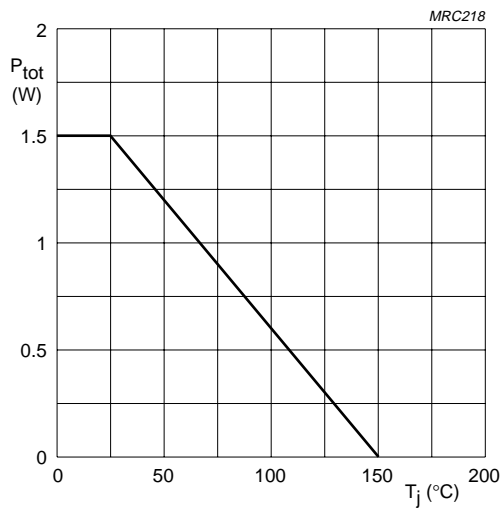
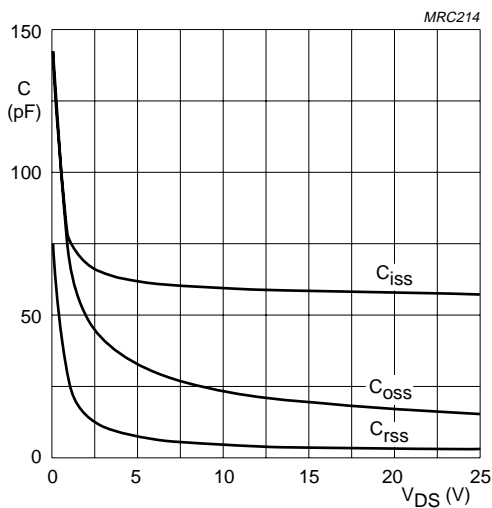


Fig.4 Power derating curve.

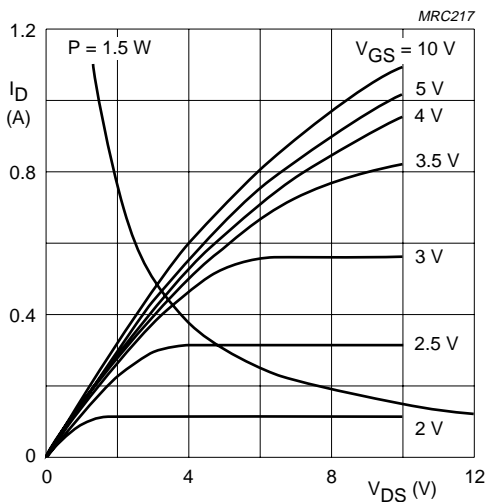


V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage, typical values.

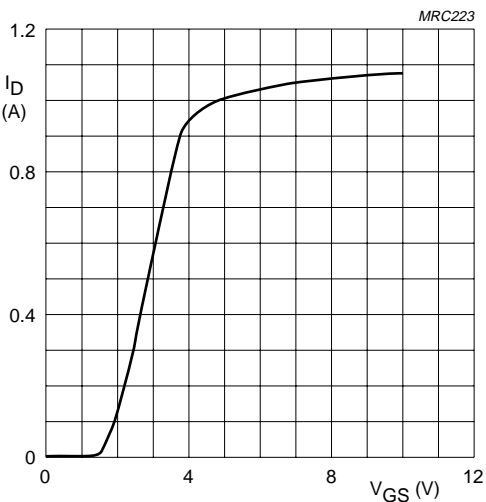
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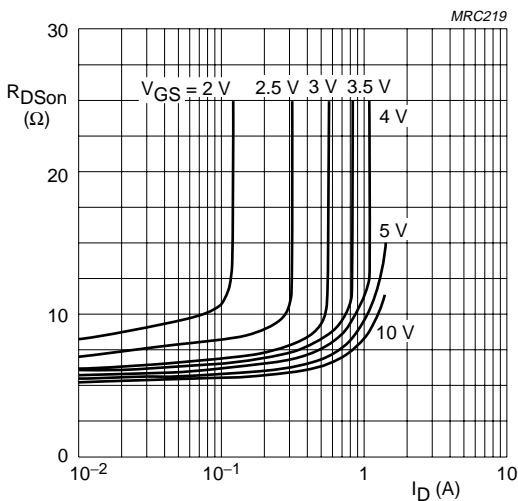
$T_j = 25^\circ\text{C}$.

Fig.6 Typical output characteristics.



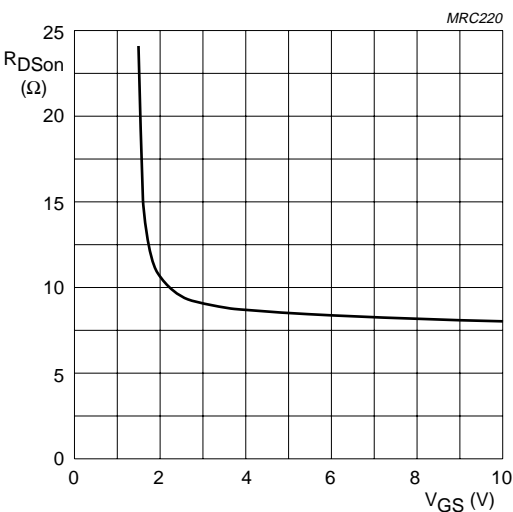
$V_{DS} = 10$ V; $T_j = 25^\circ\text{C}$.

Fig.7 Typical transfer characteristics.



$T_j = 25^\circ\text{C}$.

Fig.8 Drain-source on-resistance as a function of drain current, typical values.

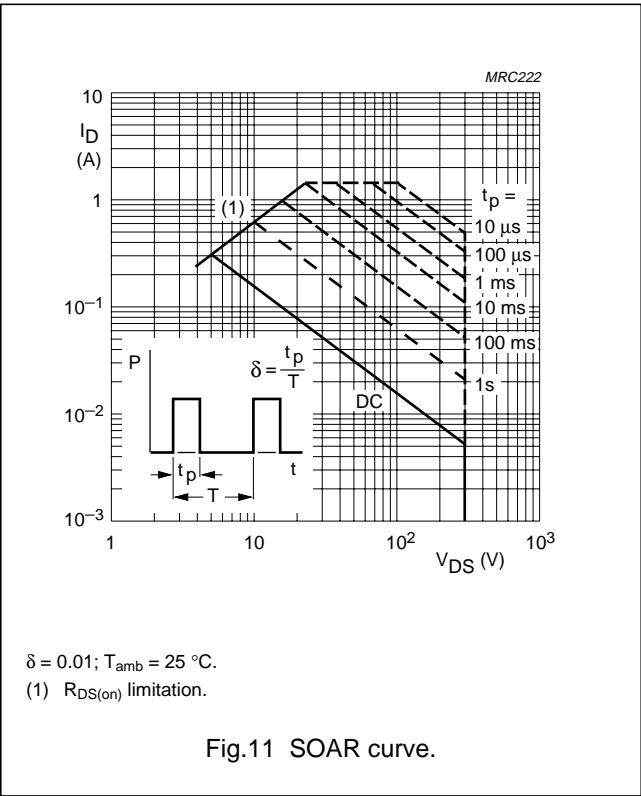
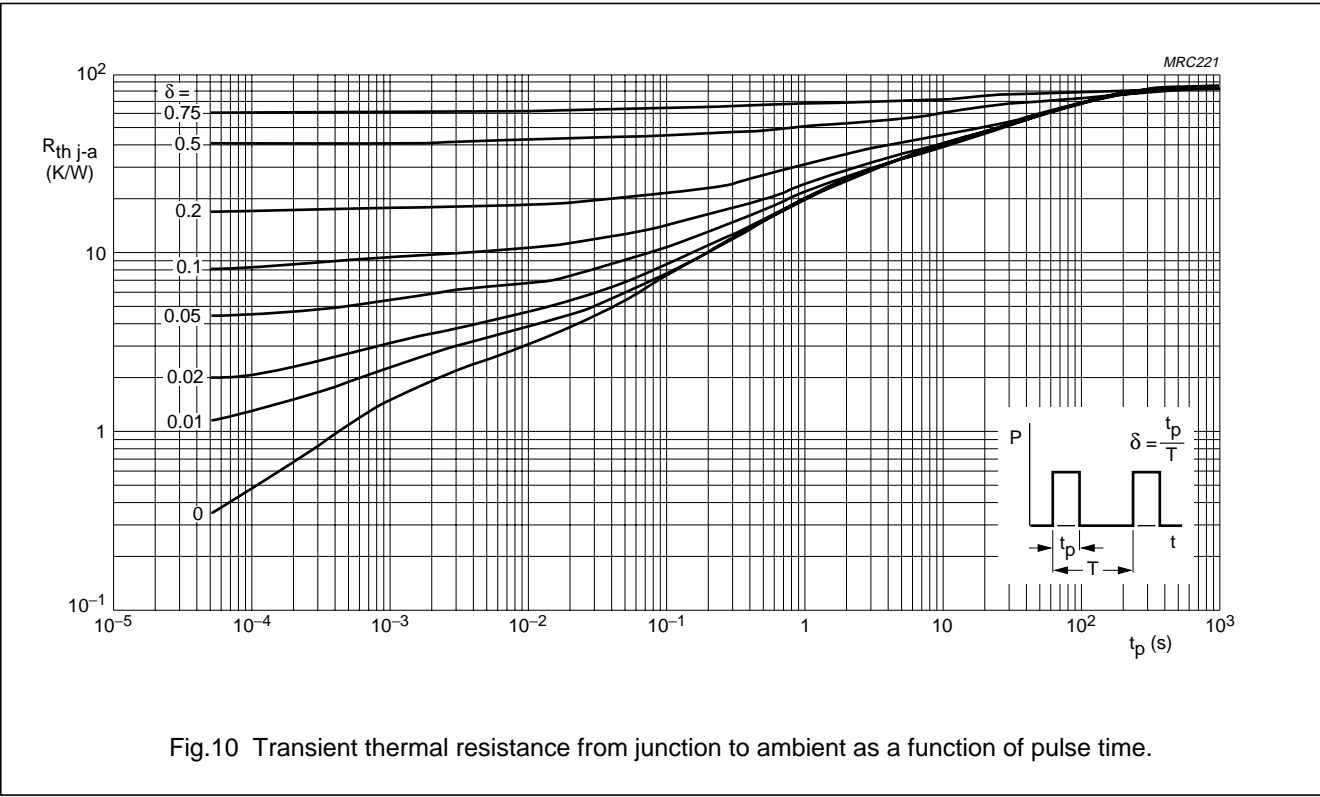


$V_{DS} = 100$ mV; $T_j = 25^\circ\text{C}$.

Fig.9 Drain-source on-resistance as a function of gate-source voltage, typical values.

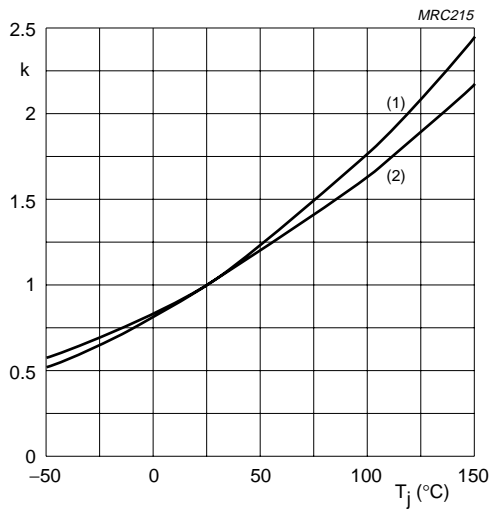
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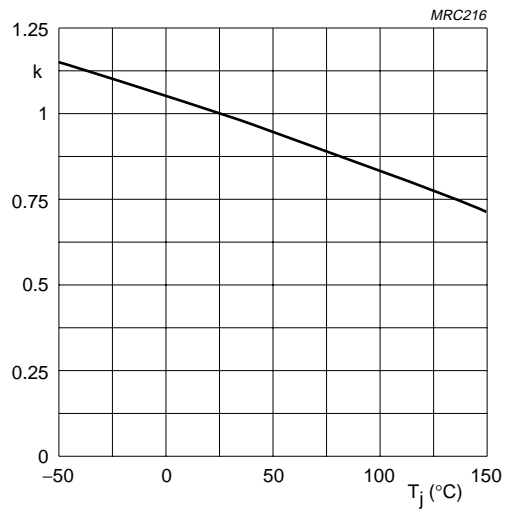
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$$k = \frac{R_{DS(on)} \text{ at } T_j}{R_{DS(on)} \text{ at } 25^\circ\text{C}}$$

Typical $R_{DS(on)}$;
(1) $I_D = 250 \text{ mA}$; $V_{GS} = 10 \text{ V}$.
(2) $I_D = 20 \text{ mA}$; $V_{GS} = 2.4 \text{ V}$.

Fig.12 Temperature coefficient of drain-source on-resistance.



$$k = \frac{V_{GS(th)} \text{ at } T_j}{V_{GS(th)} \text{ at } 25^\circ\text{C}}$$

Typical $V_{GS(th)}$ at 1 mA.

Fig.13 Temperature coefficient of gate-source threshold voltage.

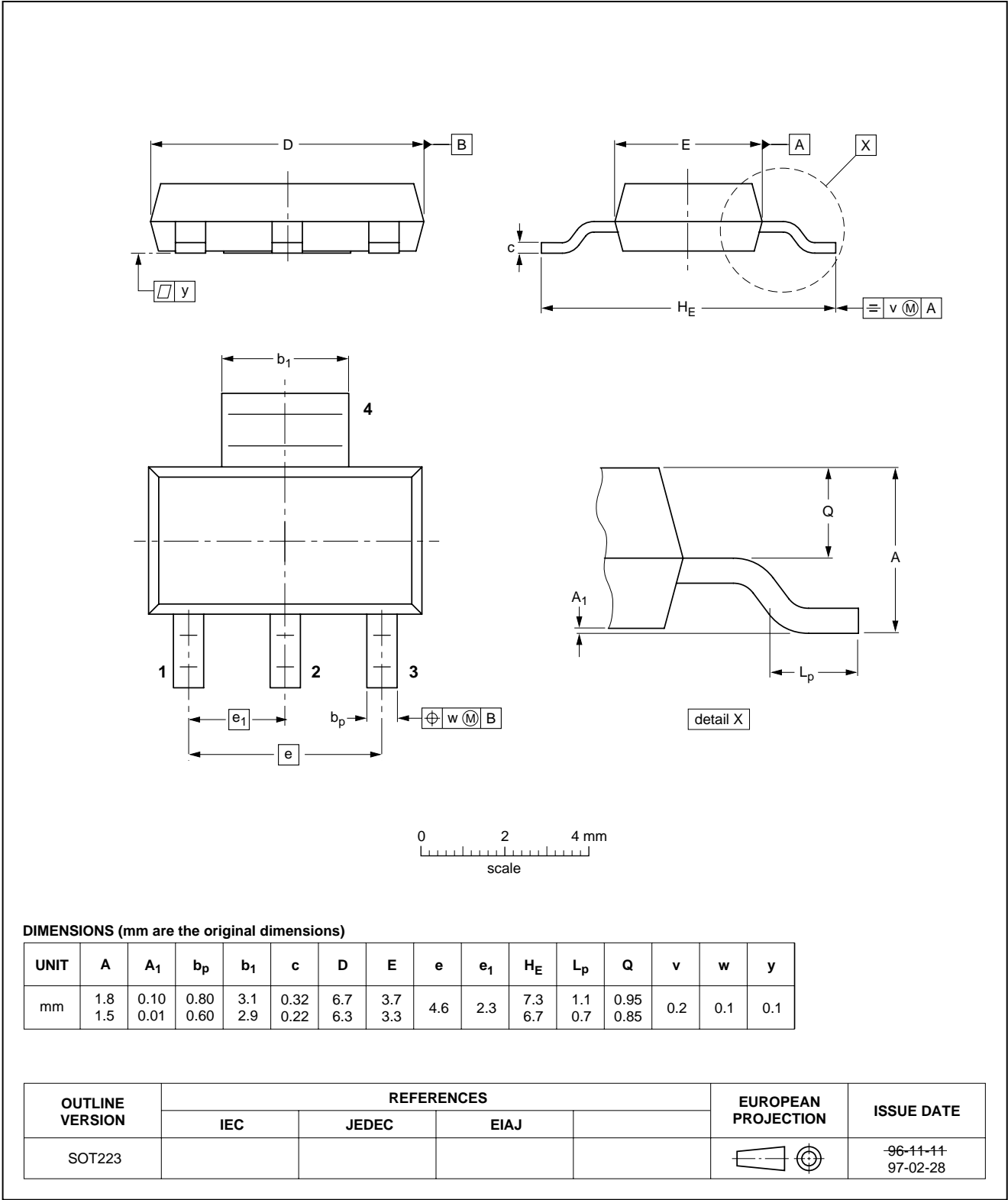
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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BSP130**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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